

FIG. 2

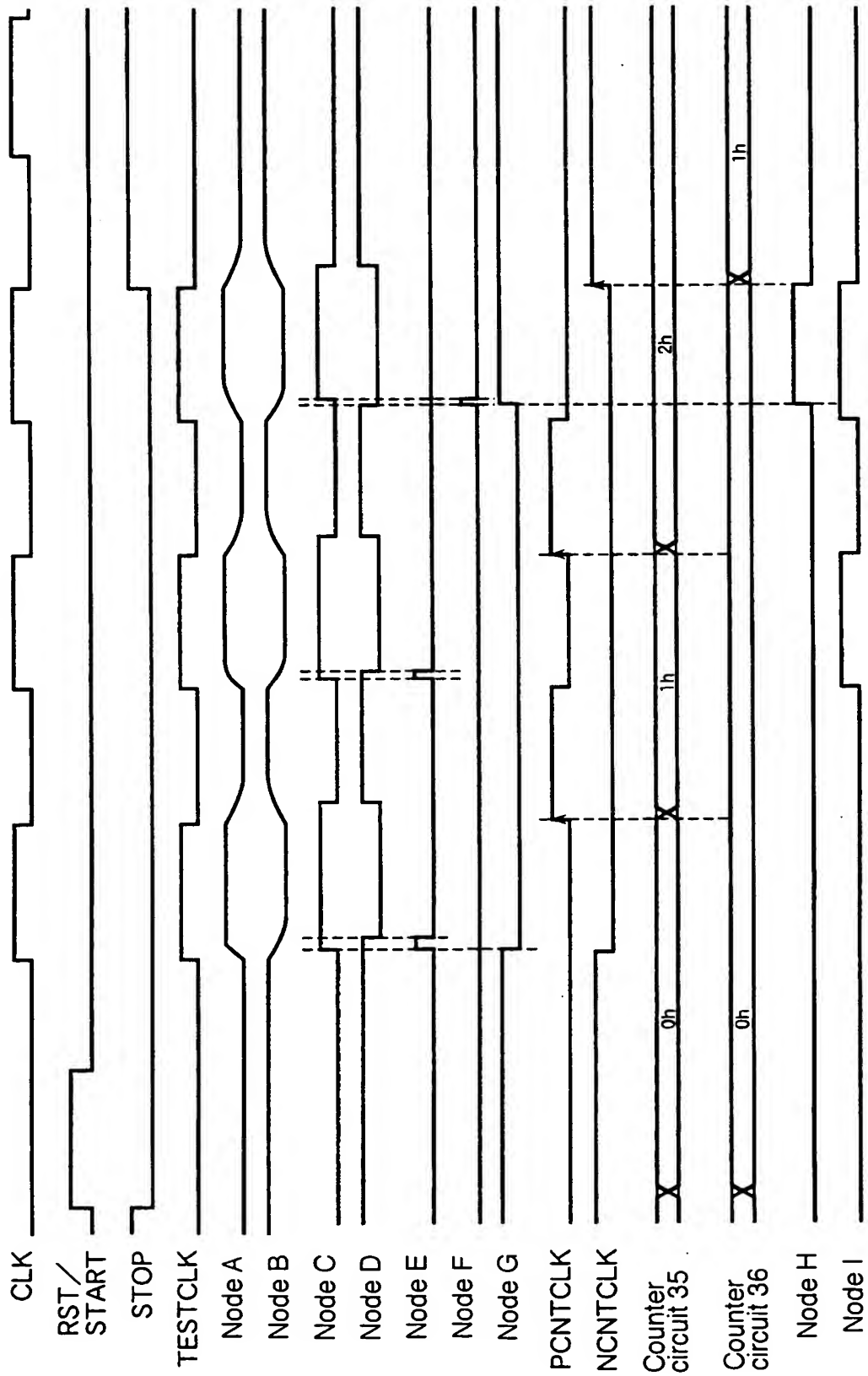


FIG. 3

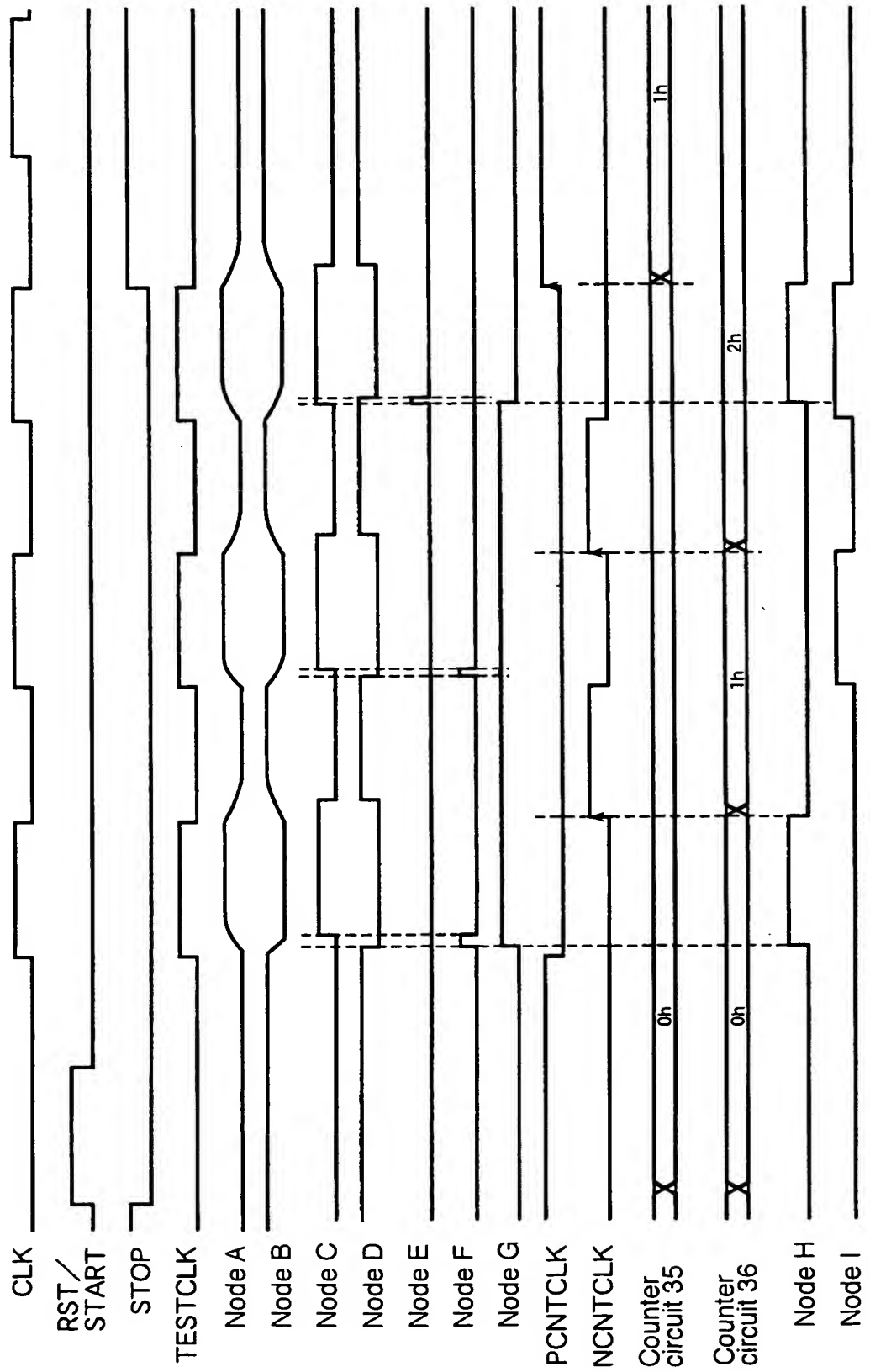


Figure 1 is a block diagram of a PWM control circuit 10. The circuit is divided into several functional blocks:

- PWM Input Section (20):** This section receives a PWM input signal and generates a PWM output. It contains two selection decode circuits (31 and 32) and four PMOS transistors (P1, P2, P3, P4) and four NMOS transistors (N1, N2, N3, N4). The PMOS transistors are connected to a common source (10a) and the NMOS transistors are connected to a common sink (10b). The PWM output is taken from the common source (10a).
- Counter Section (30):** This section includes two counter circuits (33 and 34) and a logic section (40). The counter circuit 33 is connected to the PWM input and the counter circuit 34 is connected to the PWM output. The logic section (40) contains several logic gates (35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45) and three D flip-flops (DFF1, DFF2, DFF3).
- Control Signals:** The circuit is controlled by TESTCLK, RST/START, and CLK signals. TESTCLK is connected to the counter circuits and the logic section. RST/START is connected to the D flip-flops. CLK is connected to the logic section.